

MC10H680, MC100H680

4-Bit Differential ECL Bus to TTL Bus Transceiver

Description

The MC10H/100H680 is a dual supply 4-bit differential ECL bus to TTL bus transceiver. It is designed to allow the system designer to no longer be limited in bus speed associated with standard TTL busses. Using a differential ECL Bus will increase the frequency of operation and increase noise immunity.

Both the TTL and the ECL ports are capable of driving a bus. The ECL outputs have the ability to drive $25\ \Omega$, allowing both ends of the bus line to be terminated in the characteristic impedance of $50\ \Omega$. The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads.

The ECL output levels are V_{OH} approximately equal to -1.0 V and V_{OL} cutoff equal to -2.0 V (V_{TT}). When the ECL ports are disabled both $EIOx$ and $EIOxB$ go to the V_{OL} cutoff level. The ECL input receivers have special circuitry which detects this disabled condition, prevents oscillation, and forces the TTL output to the low state. The noise margin in this disabled state is greater than 600 mV. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The control pins (EDIR and ECEB) of the 10H version is compatible with MECL 10H™ ECL logic levels. The control pins of the 100H version are compatible with 100K levels.

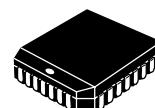
Features

- Differential ECL Bus ($25\ \Omega$) I/O Ports
- High Drive TTL Bus I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins
- Pb-Free Packages are Available*



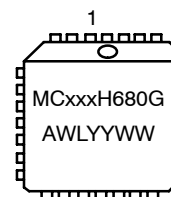
ON Semiconductor®

<http://onsemi.com>



PLCC-28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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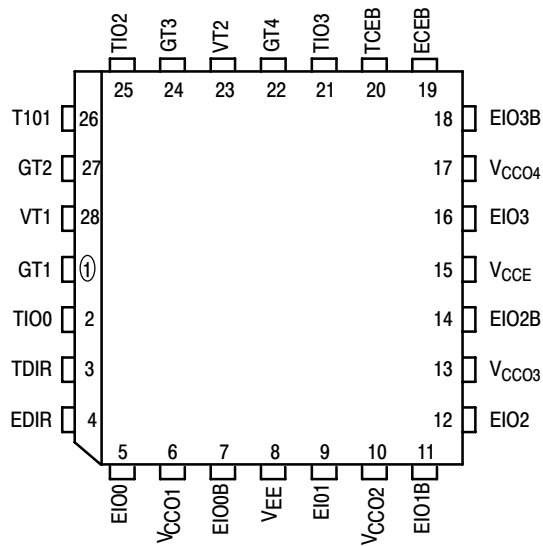


Figure 1. Pinout: PLCC-28 (Top View)

Table 1. PIN DESCRIPTIONS

Pin	Symbol	Function
1	GT1	TTL Ground 1
2	TIO0	TTL I/O Bit 0
3	TDIR	TTL Direction Control
4	EDIR	ECL Direction Control
5	EIO0	ECL I/O Bit 0
6	VCC01	ECL V _{CC} 1 (0 V) – Outputs
7	EIO0B	ECL I/O Bit 0 Bar
8	V _{EE}	ECL Supply (-5.2/-4.5 V)
9	EIO1	ECL I/O Bit 1
10	VCC02	ECL V _{CC} 2 (0 V) – Outputs
11	EIO1B	ECL I/O Bit 1 Bar
12	EIO2	ECL I/O Bit 2
13	VCC03	ECL V _{CC} 3 (0 V) – Outputs
14	EIO2B	ECL I/O Bit 2 Bar
15	VCC04	ECL V _{CC} 4 (0 V) – Outputs
16	EIO3	ECL I/O Bit 3
17	VCC04	ECL V _{CC} 4 (0 V) – Outputs
18	EIO3B	ECL I/O Bit 3 Bar
19	ECEB	ECL Chip Enable Bar Control
20	TCEB	TTL Chip Enable Bar Control
21	TIO3	TTL I/O Bit 3
22	GT4	TTL Ground 4
23	VT2	TTL Supply 2 (5.0 V)
24	GT3	TTL Ground 3
25	TIO2	TTL I/O Bit 2
26	TIO1	TTL I/O Bit 1
27	GT2	TTL Ground 2
28	VT1	TTL Supply 1 (5.0 V)

Table 2. TRUTH TABLE

ECEB	TCEB	EDIR	TDIR	EIN	EINB	EOUT	EOUTB	TIN	TOUT	COMMENTS
H	X	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
X	H	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
L	L	H	X	H	LC			NA	H	ECL to TTL Direction
L	L	H	X	LC	H			NA	L	ECL to TTL Direction
L	L	H	X	LC	LC			NA	L	ECL to TTL Direction (L-L Condition)
L	L	X	H	H	LC			NA	H	ECL to TTL Direction
L	L	X	H	LC	H			NA	L	ECL to TTL Direction
L	L	X	H	LC	LC			NA	L	ECL to TTL Direction (L-L Condition)
L	L	L	L	NA	NA	H	LC	H		TTL to ECL Direction
L	L	L	L	NA	NA	LC	H	L		TTL to ECL Direction

TDIR – Direction Control TTL Levels
 EDIR – Direction Control ECL Levels
 TCEB – Chip Enable Bar Control TTL Levels
 H – HIGH
 L – LOW
 LC – ECL Low Cutoff (V_{TT} = -2.0 V)
 X – Don't Care
 Z – High Impedance

ECEB – Chip Enable Bar Control ECL Levels
 TIN – TTL Input
 TOUT – TTL Output

EIN – ECL Input
 EINB – ECL Input Bar
 EOUT – ECL Output
 EOUTB – ECL Output Bar

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Table 3. MAXIMUM RATINGS

Parameter	Symbols	Rating	Unit
Power Supply Voltage	V_{EE} (ECL)	-8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	-0.5 to +7.0	Vdc
Input Voltage	V_I (ECL) V_I (TTL)	0.0 to V_{EE} -0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mAdc
Output Source Current Surge	I_{out} (ECL)	200	mAdc
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. DC CHARACTERISTICS, ECL $V_{CCT} = +5.0\text{ V} \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$ (10H Version);
 $V_{EE} = -4.2\text{ V to } -5.5\text{ V}$ (100H Version)

Symbol	Parameter	Condition	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit
			Min	Max	Min	Max	Min	Max	
I_{EE}	Supply Current/ECL			-110		-110		-110	mA
I_{INH}	Input HIGH Current			255		175		175	μA
I_{INL}	Input LOW Current		0.5		0.5		0.3		μA
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	25 Ω to -2.1 V	-1100 -2.1	-840 -2.03	-1100 -2.1	-810 -2.03	-1100 -2.1	-735 -2.03	mV V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 10H DC CHARACTERISTICS (CONTROL INPUTS ONLY), ECL $V_{CCT} = +5.0 \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$

Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit
		Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1070 -1950	-735 -1450	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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Table 6. 100H DC CHARACTERISTICS (CONTROL INPUTS ONLY), ECL $V_{CCT} = +5.0 \pm 10\%$, $V_{EE} = -4.2 \text{ V to } -5.5 \text{ V}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit
		Min	Max	Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	-1475	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. DC CHARACTERISTICS, TTL $V_{CCT} = +5.0 \text{ V} \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$ (10H Version);
 $V_{EE} = -4.2 \text{ V to } -5.5 \text{ V}$ (100H Version)

Symbol	Parameter	Condition	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	Standard Input		2.0		2.0		2.0		Vdc
V_{IL}	Standard Input			0.8		0.8		0.8	
V_{IK}	Input Clamp	$I_{IN} = -18 \text{ mA}$		-1.2		-1.2		-1.2	Vdc
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0 \text{ mA}$	2.5		2.5		2.5		V
	Output HIGH Voltage	$I_{OH} = -15 \text{ mA}$	2.0		2.0		2.0		
V_{OL}	Output LOW Voltage	$I_{OL} = 48 \text{ mA}$		0.55		0.55		0.55	V
I_{IH}^*	TTL (Input HIGH)	$V_{in} = 2.7 \text{ V}$		20		20		20	μA
	TTL (Input HIGH)	$V_{in} = 7.0 \text{ V}$		100		100		100	
I_{IL}^*	TTL (Input LOW)	$V_{in} = 0.5 \text{ V}$		-0.6		-0.6		-0.6	mA
I_{CCL}	Supply Current			75		75		75	mA
I_{CCH}	Supply Current			70		70		70	mA
I_{CCZ}	Supply Current			70		70		70	mA
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0 \text{ V}$	-100	-225	-100	-225	-100	-225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*TTL Control Inputs only

Table 8. DC (I/O CHARACTERISTICS ONLY), TTL

Symbol	Parameter	Condition	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit
			Min	Max	Min	Max	Min	Max	
I_{IH}/I_{OZH}	Output Disable	$V_{OUT} = 2.7 \text{ V}$		70		70		70	μA
I_{IL}/I_{OZL}	Current	$V_{OUT} = 0.5 \text{ V}$		200		200		200	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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Table 9. ECL TO TTL DIRECTION / AC TEST

Symbol	Parameter	Waveforms	Condition	T _A = 0°C		T _A = 25°C		T _A = 75°C		Unit
				Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay to Output	2, 4	C _L = 50 pF	2.7	4.8	2.7	4.8	2.7	4.8	ns
t _{PZH} t _{PZL}	ECEB to Output Enable Time	2, 5, 6	C _L = 50 pF	3.5 3.5	6.5 6.0	3.5 3.5	6.5 6.0	3.7 3.7	6.7 6.4	ns
t _{PHZ} t _{PLZ}	ECEB to Output Disable Time	2, 5, 6	C _L = 50 pF	3.5 3.5	8.6 6.5	3.5 3.5	8.6 6.5	3.7 3.7	8.8 7.3	ns
t _{PZH} t _{PZL}	TCEB to Output Enable Time	2, 5, 6	C _L = 50 pF	5.7 5.4	7.7 6.9	5.7 5.4	7.7 6.9	5.9 5.9	7.9 7.4	ns
t _{PHZ} t _{PLZ}	TCEB to Output Disable Time	2, 5, 6	C _L = 50 pF	4.0 4.0	8.5 5.8	4.1 4.2	8.4 6.0	4.2 4.7	8.3 6.5	ns
t _r /t _f	1.0 to 2.0 Vdc	3	C _L = 50 pF	0.4	1.5	0.4	1.5	0.4	1.5	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 10. TTL TO ECL DIRECTION / AC TEST

Symbol	Parameter	Waveforms	Condition	T _A = 0°C		T _A = 25°C		T _A = 75°C		Unit
				Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay to Output	1, 4	25 Ω to -2.0 V	1.8	4.6	1.8	4.6	2.0	4.9	ns
t _{PLH} t _{PHL}	ECEB to Output	1, 4	25 Ω to -2.0 V	2.9	5.1	3.0	5.2	3.4	5.7	ns
t _{PLH} t _{PHL}	TCEB to Output	1, 4	25 Ω to -2.0 V	3.4	6.3	3.5	6.6	3.8	7.4	ns
t _r /t _f	Output Rise/Fall Time 20% - 80%	1, 3	25 Ω to -2.0 V	1.0	3.4	1.0	3.4	1.0	3.4	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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CONTROL INPUTS

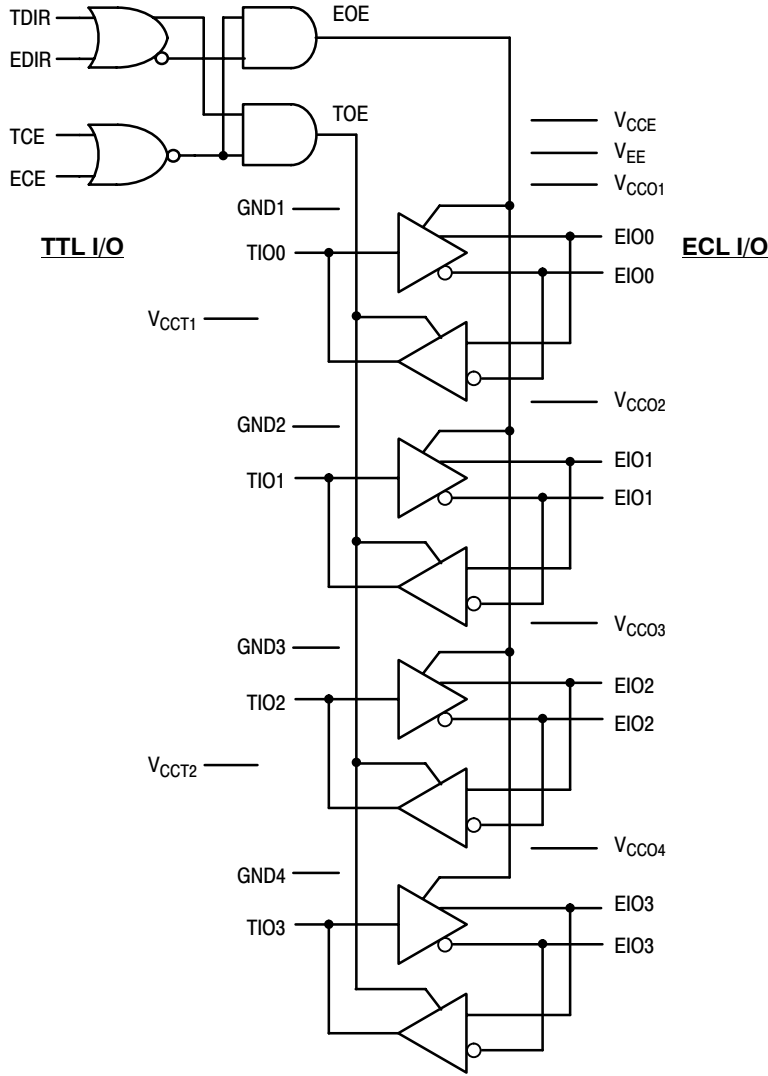


Figure 2. Block Diagram

SWITCHING CIRCUIT

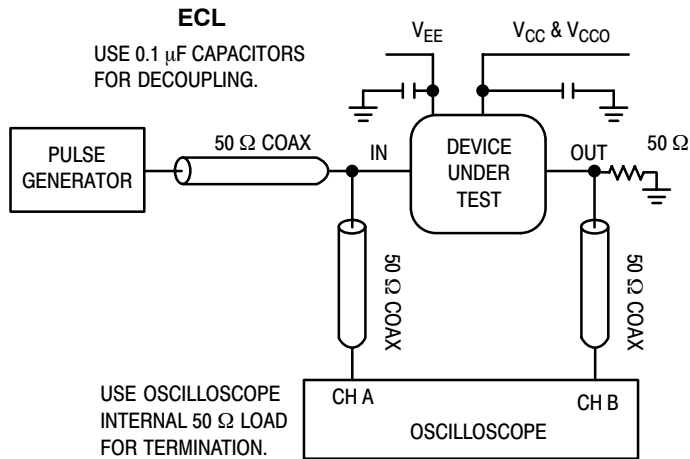


Figure 3. Switching Circuit ECL

TTL

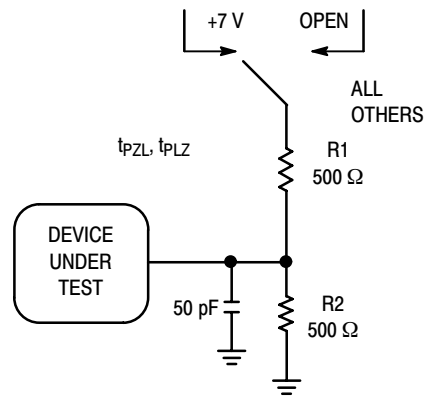


Figure 4.

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WAVEFORMS

ECL/TTL

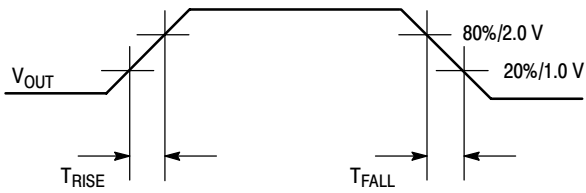


Figure 5. WAVEFORMS: Rise and Fall Times

ECL/TTL

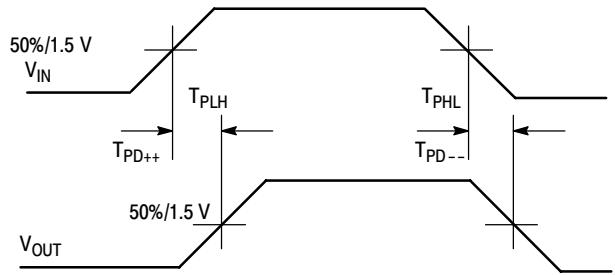


Figure 6. Propagation Delay – Single Ended

TTL

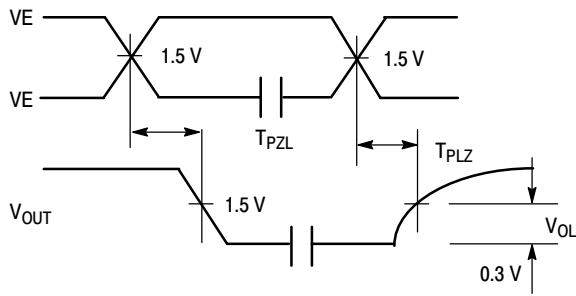


Figure 7. 3-State Output Low Enable and Disable Times

TTL

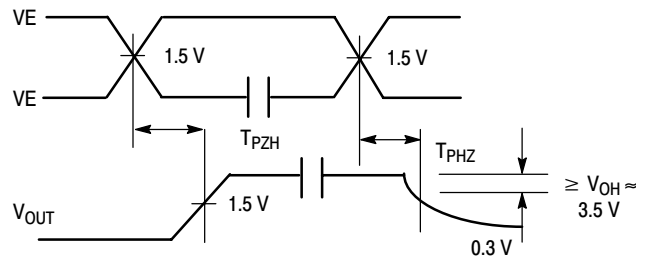


Figure 8. 3-State Output High Enable and Disable Times

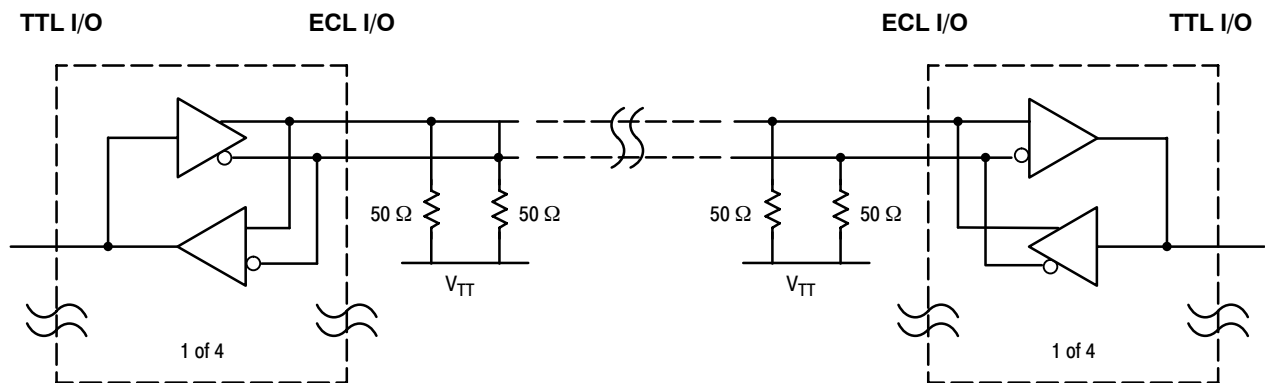


Figure 9. ECL I/O Link Application Recommended Termination
(Directional Control Intentionally Excluded)

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ORDERING INFORMATION

Device	Package	Shipping†
MC10H680FN	PLCC-28	37 Units / Rail
MC10H680FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC10H680FNR2	PLCC-28	500 / Tape & Reel
MC10H680FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel
MC100H680FN	PLCC-28	37 Units / Rail
MC100H680FNG	PLCC-28 (Pb-Free)	37 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

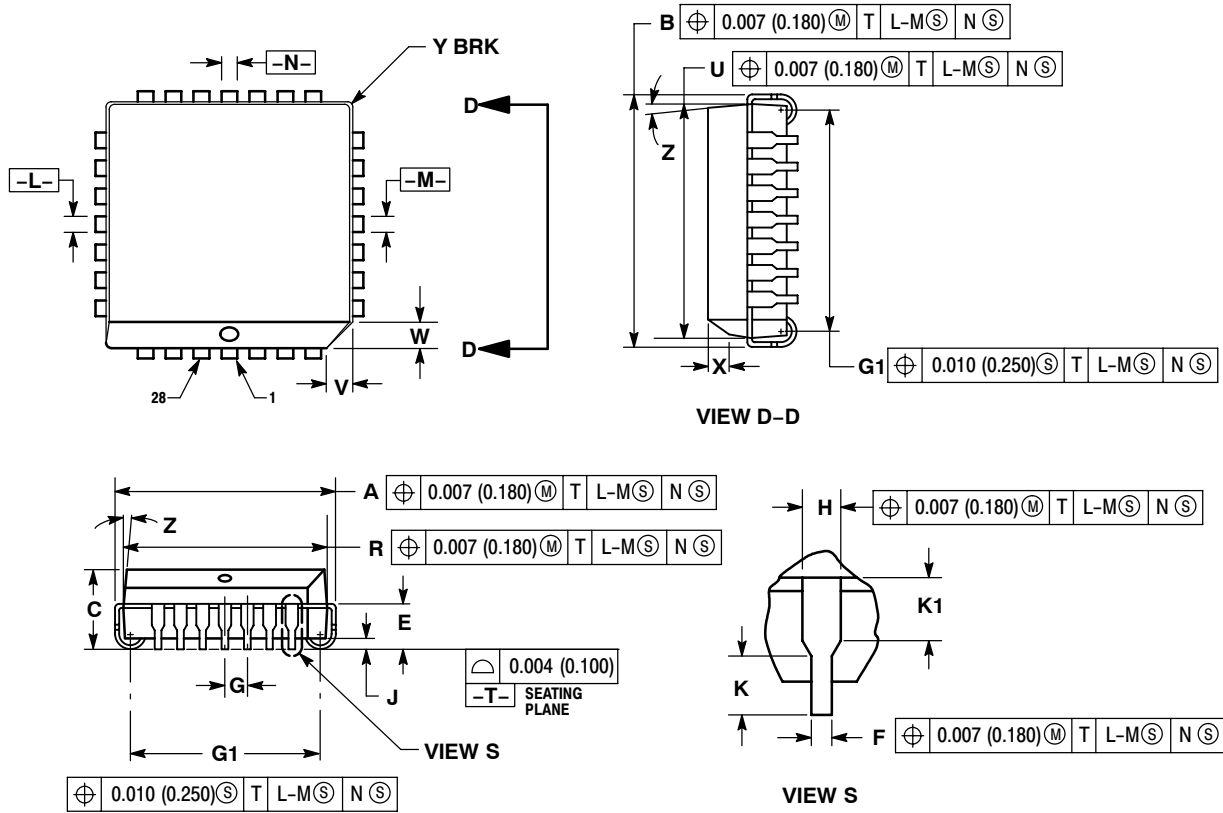
Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E




NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE BOTTOM MAY BE SMALLER THAN THE PACKAGE TOP BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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